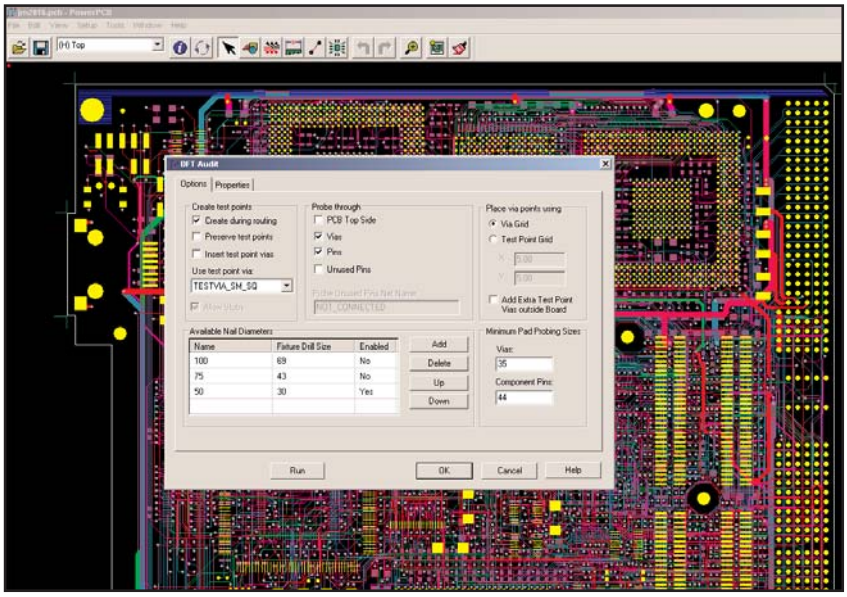
DFT Audit

PCB Layout

DATASHEET



DFT Audit reduces costly design iterations and ensures the testability of your designs before fabrication

Overview

DFT Audit is a design-for-test (DFT) option for PADS® Layout. This embedded tool allows you to perform analysis and verification as well as testpoint coverage and reporting before you release a board for fabrication. DFT Audit enables you to consider design-for-test criteria earlier in your product design cycle by performing testability analysis during PCB and advanced package design.

DFT Audit uses tools specifically developed for programming in-circuit test equipment. This guarantees 100% testability for all nets on your board and helps ensure accurate testability prior to fabrication, thus saving time and money from being spent on needless prototypes. The result is decreased time to market and improved design performance. You can back-annotate data from the Audit algorithms directly to the database or review the data through separate report files before back annotating.

Major product features

- Provides advanced verification of PCB productivity
- Supports complex testpoint-keepout areas
- Performs batch and interactive DRC checks
- Generates testpoint coverage reports for design review
- Ensures 100% testpoint coverage
- Shortens time-to-volume production
- Maximizes product quality and performance
- Decreases costly revisions
- Ensures design integrity

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Testpoint Assignment

DFT Audit uses the power of PADS® AutoRouter to insert testpoints during normal route passes, converting existing vias and pads to testpoints, or adding necessary testpoints based on your rules. PADS AutoRouter can even be instructed to perform iterative passes with decreasing probe sizes, thus maximizing testpoint coverage.

Designing for Test

DFT Audit ensures the integrity of your designs. Features within PADS® Layout support manual test-point insertion and testpoint locking. Through the use of reserved attributes, probe-size information can be passed back and captured automatically in the database. This helps to preserve test fixtures by maintaining previous testpoint locations and associated probe sizes throughout the lifecycle of the design. Graphical indicators make it easy to identify test-point locations visually.

You can control testpoint rules to mirror the rules used in the Automated Test Engineering (ATE) environment. These rules include probe-to-probe, probe-to-component, and probe-to-board clearances.

You can also drive testpoint requirements directly from the DxDesigner™ schematic-capture environment. Furthermore, you can define different probe types, to be included or excluded, through a simple user interface, enabling you to simulate a multi-pass environment.

DFT Audit rules can also be used to verify manual testpoint insertion. This ensures that you are using the same rules and criteria during both batch and interactive operations. Using traditional DRC-style functionality, you have the option of checking a "windowed area," the entire PCB, or an advanced package. Coupled with the ability to specify and recognize complex testpoint-keepout areas, you can simulate the exact requirements that ATE engineers use prior to committing the design to fabrication.

At any time, a comprehensive testpoint coverage report can be generated for design review.

Summary

By leveraging the knowledge base that already exists in the ATE environment, you can implement design-for-test technology directly in the engineering environment. The advanced functionality of DFT Audit allows you to design and implement testability directly into your PCBs or advanced package based on user, product, or corporate defined test strategies. This optimizes design efficiency and effectiveness.

By incorporating DFT Audit into your design process, you can dramatically decrease time-to-volume production, reduce costs, and improve product quality.

PADS Layout Options

- Advanced Packaging Toolkit
- Advanced Rule Set (ARS)
- Analog Toolkit
- Assembly Variants
- Cluster Placement
- Database Viewer
- DFF Audit
- PADS Router interactive route editor)
- PADS Router HSD
- IDF Link
- Physical Design Reuse (PDR)

Visit our website at www.mentor.com/pads

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