



HDL Designer
HDL Author
HDL Detective

HDL Designer Series™ v2006.1 Product Feature Matrix

Product Feature				Special Notes
Conversion from RTL to Graphics (Editable)				
HDL File Import	X	X	X	
Block Diagram	X	X	X	Creates Editable Graphics that will be used to generate RTL
Interface Based Design (IBD)	X	X	X	
State Diagram	X	X	X	
Flow Chart	X	X	X	
Symbol with Tabular IO	X	X	X	
Moduleware Libraries	X	X		
External IP Generator Integration	X	X		Xilinx Core Generator & Altera MegaWizard
Static Analysis				
RTL analysis	X	X		Xilinx, RMM, Altera, Essentials
Code Quality Scoring	X	X		
Visualization / Rendering				
Block Diagram	X	X	X	HDL Detective: Edits to Visualization but No Logical Edits
Interface Based Design (IBD)	X	X	X	
State Diagram	X	X	X	
Flow Chart	X	X	X	
Documentation Generation				
OLE	X	X	X	Windows only
HTML	X	X	X	
Printing	X	X	X	
Graphics Export (SVG/JPG/PNG)	X	X	X	
Languages and Platforms				
Batch Mode Operation	X	X	X	
UNIX (32 & 64 bit - Solaris & HP-UX)	X	X	X	Single executable for 32/64 bit
Windows (NT, 2000, XP)	X	X	X	
Linux (Redhat/SuSE)	X	X	X	Redhat Enterprise 4.0
VHDL	X	X	X	
Verilog95, Verilog 2001	X	X	X	
Mixed-HDL	X	X	X	
C/C++ Model Support	X	X		
Design Management				
Multiple Design View Support	X	X	X	
Data Management	X	X		[L] Limited; e.g. no checks, reporting or component browsing
Project Manager	X	X	X	
Non-HDL Data	X	X		Any files such as documents, scripts, etc.
Version Management	X	X	X	RCS & CVS Included with HDS
Version Management Integration	X	X	X	Rational ClearCase, Synchronicity DesignSync, Microsoft VSS, ClioSoft SoS, Merant PVCS
Synthesis Tool Integration	X	X		LeonardoSpectrum, Precision Synthesis, Design Compiler, Synplify/Synplify-Pro
Digital Simulation Tool Integration	X	X		Modelsim, NC-Sim, VCS/VCSi
FPGA Vendor Flows	X	X		Xilinx ISE, Altera QuartusII
FPSOC Tool Integration	X	X		Xilinx Platform Studio, Altera SOPC Builder
Custom Tools and Flows	X	X		
Editors				
Block Diagram	X	X	N	[N] No logical changes allowed
Interface Based Design (IBD)	X	X	N	[N] No logical changes allowed
State Diagram	X	X	N	[N] No logical changes allowed
Algorithmic State Machine (ASM)	X	X	N	[N] No logical changes allowed
Flow Chart	X	X	N	[N] No logical changes allowed
Truth Table	X	X	N	[N] No logical changes allowed
Symbol with Tabular IO	X	X	N	[N] No logical changes allowed
Built-in Text editor (DesignPad)	X	X	R	[R] Read-only
External Text editor integration	X	X	R	[R] Read-only
HDL Templates	X	X		
Waveform Editor (DesignWave)	X	X	R	[R] Read-only
Simulation Analyzer				
ModelSim PE/SE	X	X		[X] Full invocation and debug support
Cadence NC-Sim	X	X		[X] Full invocation and debug support