



FEATURE	AE	ModelSim PE	ModelSim LE	ModelSim SE
DESIGN LIMITS				
SDF Back-Annotation to FPGA/ASIC Libraries	Altera Designs Only	None (unlimited)	None (unlimited)	None (unlimited)
GENERAL				
Licensing - Floating License		option	option	■
Language Neutral License		option	option	option
ASIC Sign-Off				■
Platform-Independent Compiled Database		■	■	■
32/64-Bit Cross-Compatibility				■
LANGUAGES				
VHDL	■	■		■
Verilog	■	■	■	■
Mixed Language		option	option	option
SystemC			■	option
System Verilog – Phase 1 (no Testbenches or Assertions)			■	■
PSL VHDL		option	option	option
Analog/Mixed-Signal				option (Advance MS product)
VHDL FLI				■
DEBUG				
Enhanced Dataflow Window (includes ChaseX)		option	■	■
C Debugger			option (with SystemC)	■
Extra Standalone Viewers		option	option	option
Multiple Waveform Windows				■
Code Coverage		option	option	■
Waveform Compare		option	■	■
User-Customizable GUI (via Tk)				■
SIMULATION				
Single-Kernel Simulation Engine		■	■	■
Verilog Global Optimization				■
Verilog Gate Acceleration				■
Performance Analyzer				■
Separate Elaborate Option				■
VCD Re-Simulation				■
Checkpoint & Restore				■
SWIFT Interface / SmartModels		option	option	■
Synopsys Hardware Modeler Support				■
PLATFORM SUPPORT				
32-Bit OS Support	Windows 98/NT/ME/2000/XP, Linux	Windows 98/NT/ME/2000/XP	Linux	AIX, HP-UX, Linux + Solaris, Windows 98/NT/ME/2000/XP
64-Bit OS Support				AIX, Linux (Itanium-2), HP-UX, Solaris