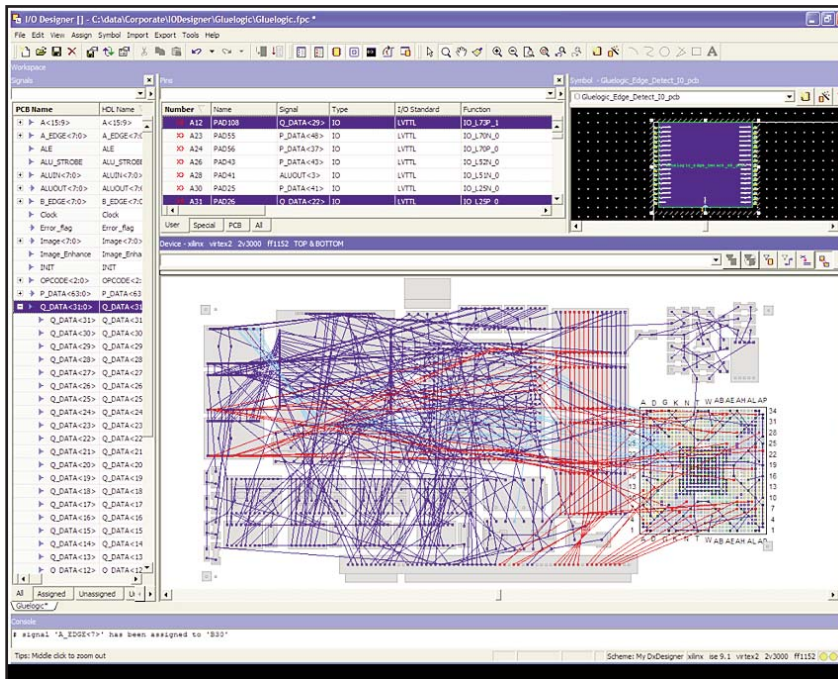


# PADS I/O Designer

Optimizing FPGA on PCB Systems Design

FPGA – PCB  
Concurrent Design

D A T A S H E E T



*PADS I/O Designer's graphical and spreadsheet based design environment.*

## Major product features:

- Eliminates re-spins due to FPGA-PCB interface synchronization errors
- Reduces design cycle time by as much as one week for every 500 FPGA pins on the PCB
- Follows all major FPGA vendor rules for correct-by-construction I/O assignments
- Views and optimizes single or multiple FPGAs in the context of your PADS Layout database
- Reduces PCB trace lengths and propagation delays

## Overview

FPGA usage is pervasive across a variety of electronic products. The flexibility, performance and quick turn availability of FPGA devices have made these “liquid silicon” devices the ideal choice to gain a time-to-market and cost advantage over traditional off-the-shelf & ASIC components in product design. However, power and flexibility come with increased complexity.

The complexity of FPGA usage for system design is primarily manifest through the FPGA package – PCB interface although the simple challenge of creating a legal FPGA pin assignment currently requires FPGA device/package specific expertise. The challenges of synchronizing PCB symbol and schematic definitions with FPGA vendor and the FPGA HDL design & synthesis files, often forces design teams to freeze the FPGA-PCB interface early in the system design process. By doing this they lose the opportunity to use the flexibility of the FPGA interface to optimize the PCB design for routing congestion, performance, reliability, PCB Manufacturing costs, PCB Manufacturing yield and ultimately product profit margin.

To address these complexity issues and provide designers with automated functionality to synchronize their FPGA and PCB design processes, and, enable optimization at the system level, Mentor Graphics has developed PADS I/O Designer.

## Intelligent FPGA Pin Assignment

The PADS I/O Designer interface provides correct-by-construction, drag and drop functionality that enables FPGA designers to easily create legal FPGA pins assignments. Mentor Graphics partnerships with the major FPGA vendors combined with leading edge rules-based technology provides FPGA vendor-specific device expertise that extends down to every FPGA pin. Packaged with signal and pin sorting and filtering capabilities along with powerful signal-to-FPGA pin assignment methods, PADS I/O Designer delivers productivity essential to effectively manage the complexity of modern FPGA-PCB interface designs.

### Avoiding Design Re-spins

FPGA-PCB design process synchronization is critical for avoiding time consuming re-spins created by FPGA-PCB interface errors. To avoid these costly re-spins, designers spend time comparing PCB symbols and schematics to the FPGA vendor's rules, the FPGA synthesis tool and the FPGA HDL design, one pin at a time. For true concurrent design, PADS I/O Designer supports bi-direction flow synchronization allowing design interface changes from any point in the complete FPGA + PCB design flow and communicated quickly across interface boundaries.

PADS I/O Designer provides a complete solution enabling true concurrent FPGA-PCB design with your existing DxDesigner-PADS Layout PCB flow and a variety of FPGA design flows:

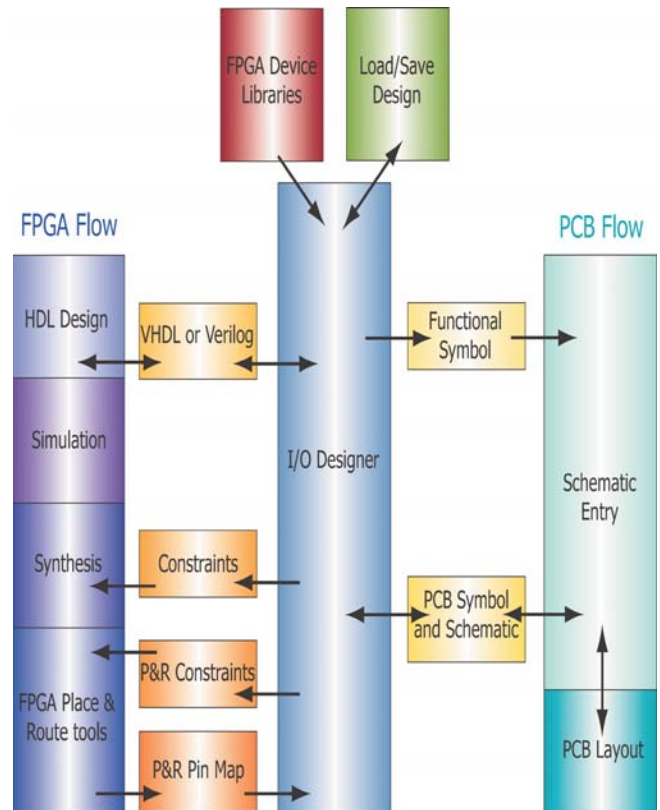
- Mentor Graphics FPGA Advantage
- Actel, Altera, Lattice & Xilinx FPGA design tools
- Synthesis tools from Synplicity and Synopsys
- Any mixture of supported EDA & FPGA Vendor tools

PADS I/O Designer automatically detects FPGA-PCB interface synchronization conflicts anywhere in the FPGA + PCB system design flow notifying you with suggested resolutions.

### PCB Optimization and Design Cycle Time Reduction

The core capabilities of PADS I/O Designer address the complexity of FPGA-PCB interface design accelerating product time-to-market and enabling the power and flexibility of FPGA devices to drive PCB optimization in a true FPGA-PCB concurrent system design flow. However, using FPGA interface flexibility for PCB optimization requires FPGA device/package specific expertise plus PCB physical design expertise.

Mentor Graphics PADS I/O Designer bridges the gap between the FPGA and PCB design domains. The resulting combination of the PADS Layout physical PCB view while adhering to all of the



*I/O Designer integrates the FPGA and PCB design flows.*

FPGA device/package specific rules assures correct-by-construction pin swaps and optimization of those pin assignments in the context of the complete PCB.

Additional capabilities are available for PADS I/O Designer that automate the PCB optimization process for one or multiple FPGA devices on the same PCB system design. Extending the PCB optimization capabilities to the logical extreme, PADS I/O Designer may be upgraded to provide simultaneous PCB optimization across all of the FPGA devices on your PCB system design. The resulting competitive advantage has been demonstrated by early adopters to be as great as a 50% reduction in your total design cycle time

### Hardware Platforms

- PC

### Operating Systems

- Windows 2000, XP

### System Requirements

- 1 GB free disk space
- 512 MB system RAM recommended

### License Configuration

- Time based
- Node Locked
- FlexLM protected

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